In the Claims

Please cancel claim 1 without prejudice or disclaimer and add new claims 18-29 as follows:

18. (New) A method of making an array of thin film transistors (TFTs) comprising:

providing a substrate;

forming a plurality of gate electrodes and gate lines on the substrate, the gate lines being connected to the gate electrodes;

forming a gate insulating layer over the gate electrodes;

forming a semiconductor layer over each of the gate electrodes;

forming source and drain electrodes with a channel therebetweeen and a plurality of data lines;

forming a photo-imageable insulating layer having a dielectric constant less than about 5.0 over a substantial portion of the substrate;

forming a plurality of vias in the photo-imageable insulating layer, at least one via corresponding to a thin film transistor in the array; and

forming a plurality of pixel electrodes over the photo-imageable insulating layer, each pixel electrode contacting one of the source and drain electrodes of the thin film transistor through the at least one via;

wherein the pixel electrode on the substrate overlaps at least one of the gate and data lines whereby the pixel electrodes are insulated from the gate and data lines in the overlap area by the photo-imaged insulating layer, and

wherein the parasitic capacitance corresponding to an overlap of said each pixel electrode to one of the gate and data lines is no greater than 0.01 pF.

19. (New) The method of claim 18, wherein the photo-imageable insulating layer has a dielectric constant of less than about 3.0 over a substantial portion of the substrate.

20. (New) The method of claim 18, wherein the photo-imageable insulating layer has a thickness of about 1.5 μm in areas where the pixel electrode overlaps one of the gate and data lines.

21. (New) The method of claim 18, wherein the pixel pitch of the display is about 150 μm.

B2 cont'd

22. (New) A method of making a liquid crystal display including an array of thin film transistors (TFTs), comprising:

forming an array of semiconductor based TFTs and corresponding address lines on a substrate;

forming an organic insulating layer on the first substrate over the TFTs and address lines, the organic insulating layer having a dielectric constant of less than about 5.0;

photo-imaging the insulating layer to forming a plurality of contact holes therein; and

forming an array of pixel electrodes over the photo-imaged insulating layer so that each pixel electrode communicates with one of the TFTs through a corresponding one of the contact holes in the insulating layer,

wherein the pixel electrodes overlap at least one of the address lines thereby resulting in a high aperture display which includes a pixel aperture ratio greater than a display without such overlap and a parasitic capacitance corresponding to an overlap of one of the pixel electrodes to

one of the drain and gate lines is no greater than 0.01 pF.

23. (New) The method of claim 22, wherein the organic insulating layer has a dielectric constant of less than about 3.0.

24. (New) The method of claim 22, wherein the organic insulating layer is from about 1.0 to 2.5 μm thick.

25. (New) The method of claim 24, wherein the insulating layer is substantially transparent.

B2 cont'd

26. (New) A method of making a liquid crystal display having a substrate including an array of transistors, comprising:

forming an array of transistors and corresponding address lines on the substrate;

forming an organic insulating layer on the substrate over the transistors and gate and data lines, the organic insulating layer having a dielectric constant of less than about 5.0 and a thickness in areas thereof of at least about 1.0 μm;

photo-imaging the organic insulating layer to form a plurality of contact holes therein;

forming a plurality of pixel electrodes over the photoimaged organic insulating layer so that each pixel electrode overlaps at least a portion of at least one of the gate and data lines and communicates with one of the transistors through a corresponding one of the contact holes in the organic insulating layer; and

providing the organic insulating layer in a thickness of at least about 1.0 μm in areas thereof so that the line-pixel capacitance between at least one of the gate and data lines and an

overlapping pixel electrode sandwiching the organic insulating layer therebetween is less than about 20 fF.

27. (New) The method of claim 26, wherein the organic insulating layer has a dielectric constant of less than about 3.0 over a substantial portion of the substrate.

B2 contd

28. (New) The method of claim 26, wherein the organic insulating layer has a thickness of about 1.5 μm in areas where the pixel electrode overlaps one of the gate and data lines.

29. (New) The method of claim 26, wherein the line-pixel capacitance is less than or equal to 12 fF.